AF/2812

DOCKET NO. 94-C-096C4 (STMI01-94096) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	KUEI-WU HUANG ET AL
Serial No.	:	09/517,987
Filed	:	March 3, 2000
For	:	METHOD OF FORMING PLANARIZED STRUCTURES IN AN INTEGRATED CIRCUIT
Group No.	:	2812
Examiner	:	R.A. Booth

BOX AF
Commissioner for Patents
Washington, D.C. 20231

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APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellant for the application identified above. A check is enclosed for the $320.00 fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 77–96 are pending in the present application. Claims 77–84 and 86–96 were rejected under 35 U.S.C. § 103(a). The rejection of pending claims 77–84 and 86–96 is appealed.

STATUS OF AMENDMENTS

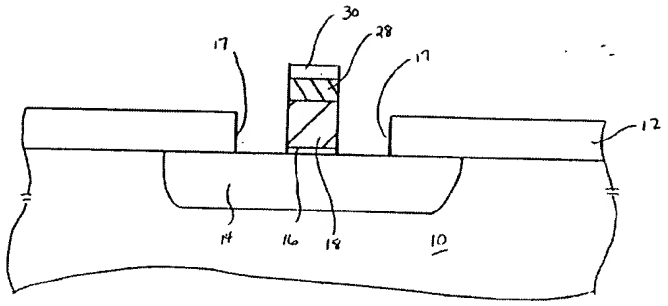
An Advisory Action mailed August 1, 2002 indicates that the amendments to the claims filed on July 17, 2002 following the final Office Action mailed May 17, 2002 will be entered for the purposes of appeal.

SUMMARY OF THE INVENTION

The present invention relates to formation of transistor structures in integrated circuits. In the present invention, an opening having substantially vertical sidewalls is etched through a field oxide 12 over a doped well 14 within a substrate 10, and a gate electrode comprising a gate

oxide 16, a an electrode comprising a polysilicon layer 18 and a silicide layer 28, and a capping layer 30 is formed within the opening:

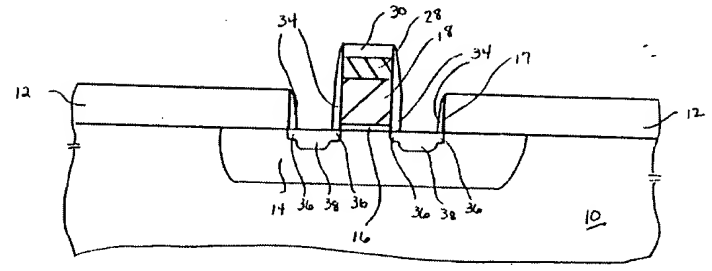
FIG. 3



Specification, Figure 3; page 9, line 14 through page 13, line 14. The polysilicon layer 18 within the gate electrode has a height above the surface of the substrate 10 that is greater than the height of the field oxide 12. Specification, page 13, lines 14–19.

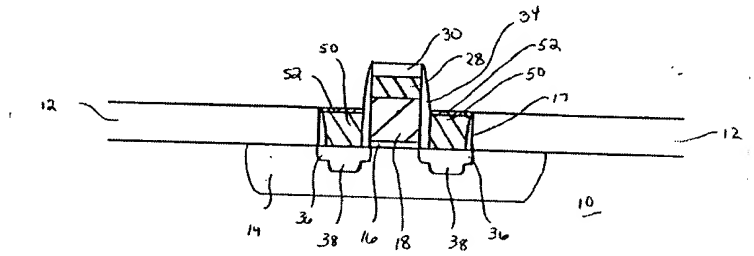
Source and drain regions are then formed adjacent the gate electrode by implanting a lightly doped region within the substrate adjacent the gate electrode, forming sidewalls 34 on the vertical surfaces of the gate electrode and the field oxide 12, and implanting a heavily doped region over lapping the light doped region, forming heavily doped source/drain regions 38 and lightly doped source drain regions 36:

FIG. 4

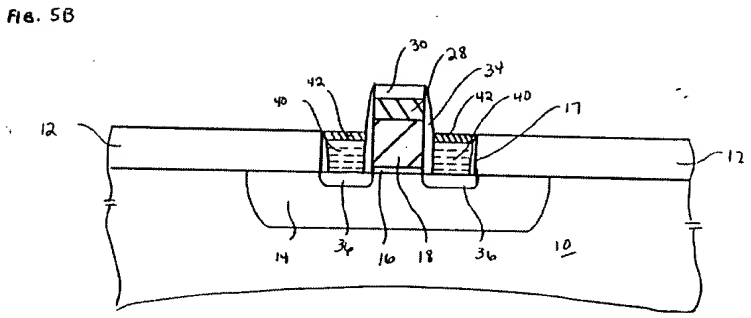


Specification, Figure 4, page 14, lines 1–12. An epitaxial layer 50 is then grown over the exposed surfaces of the substrate 10 to fill the regions over the implanted source/drain regions 36, 38 and between the sidewall spacers 34 and form raised source/drain regions 50:

FIG. 6B



Specification, Figure 6B, page 16, lines 18–20. The epitaxially grown raised source/drain regions 50 are doped to serve as heavily doped source/drain regions. In one embodiment, only lightly doped source/drain regions 36 are implanted into the substrate 10, with the heavily doped source/drain regions 40 being formed entirely above the substrate, in the epitaxially-grown raised source drain regions:



Specification, Figure 5B, page 15, lines 17–19.

ISSUES ON APPEAL

Claim 85 was rejected in the final Office Action (Paper No. 20) under 35 U.S.C. § 112, first paragraph as containing subject matter not described in the specification. However, the Advisory Action (Paper No. 23) indicates that the amendment after final overcame this rejection. Claims 77–84 and 86–96 were rejected in the final Office Action under 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,244,289 to *Pierce* in view of U.S. Patent No. 5,346,587 to *Doan et al.* The sole issue on appeal is whether claims 77–84 and 86–96 were properly rejected under 35 U.S.C. § 103.

GROUPING OF CLAIMS

Claims 77–84 and 86–96 were rejected under 35 U.S.C. § 103. For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 77–96 (all pending rejected claims); and

Group B – claims 87 and 90–91.

Groups A–B stand or fall independently. Patentability of the claims within each group is argued separately below.

DISCUSSION OF THE CITED REFERENCES

Pierce

Pierce discloses a planarized transistor structure in which a source 34 and drain 36 (depicted by not described as including both heavily doped and lightly doped portions) are contacted by conductive contacts 38 and 40 filling an opening and having an upper surface planar with the gate 28:

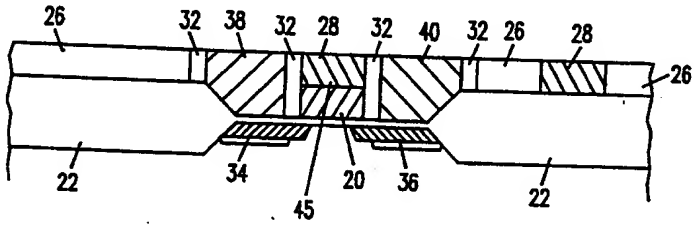


FIG. 5

Pierce, Figure 5, column 11, line 60 through column 12, line 10. *Pierce* discloses three options for forming conductive "plugs" 38 and 40:

> Following spacer formation and any desired doping modifications to the source and drain regions, the next step according to this invention is to fill the openings above the source and drain regions and planarize, if necessary, to produce the structure of FIG. 5. Several options for accomplishing this can be employed depending upon the MOSFET design. In one option, any residual gate dielectric is cleaned out of the active regions and a polysilicon layer is deposited

over the wafer. CMP is then used to planarize the surface as was previously conducted on layers 20 and 28. If the polysilicon is appropriately doped (before or after deposition), a final annealing step may then be used to diffuse the dopant uniformly through plugs 20, 28, 38, and 40 and out of plugs 38 and 40 into the single crystal silicon to form shallow source drain junctions as indicated in FIG. 5.

Alternatively, polysilicon or epitaxial single-crystal silicon may be grown by a selective CVD process on the exposed silicon in the source and drain areas only. The deposition can be terminated when the growing deposit reaches the level of the upper surface, so no additional planarization step is needed. This process requires deposition of a thin layer of dielectric (typically 0.50-0.15 μm) over the structure of FIG. 3 prior to applying the resist for mask 103. This layer remains in place through the etch and spacer formation steps such that no sections of conductive layer 28 will be exposed during the selective CVD process. If single-crystal epitaxial silicon is elected in this option, it will often be necessary to use in-situ doping during the CVD process because the heat treatment required to diffuse implant dopant through a single-crystal layer is incompatible with the shallow junctions required in modern MOSFETs.

In a third option, a barrier metal is first deposited, and then another material, such as tungsten, titanium, titanium nitride, aluminum, copper or a refractory metal silicide, is deposited as is commonly used for making contacts in conventional processes. If this option is used, the doping of the source and drain regions and the gate layers must be complete, including any implant activation anneals, prior to metal deposition. In addition, the metal layer may have to be planarized by CMP to produce the structure of FIG. 5. Alternatively, a selective CVD process for the plug metal can be used as described above, in which case no planarization is required.

Pierce et al, column 11, lines 12–59.

Doan et al

Doan et al teaches a transistor structure planarized with interconnects formed on adjacent isolation oxide regions.

ARGUMENT

Group A

Claims 77–84 and 86–96 of Group A were rejected under 35 U.S.C. § 103 as obvious over *Pierce* in view of *Doan et al.* These claims are properly grouped together and considered separately from the claims of Group B since they are subject to common grounds of rejection and contain common limitations distinguishing the claims over the cited references, and since a decision with respect to the claims of Group A may obviate the need for consideration of Group B.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d

1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

Independent claim 77 of Group A recites that the source and drain regions each include a first portion in the substrate and a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode. Similarly, independent claim 93 of Group A recites that doped regions within the substrate and doped semiconductor material on the substrate form a source and drain for a transistor, while independent claim 96 of Group A recites that doped source and drain regions extend into the substrate and within

semiconductor material on the substrate. Such a feature is not shown or suggested by the cited references.

Pierce discloses, in Figure 5, a structure in which the source and drain regions 34 and 36 are completely within the substrate, with conductive contacts or plugs 38 and 40 over the source and drain regions 34 and 36 are provided for electrically contacting the source and drain regions:

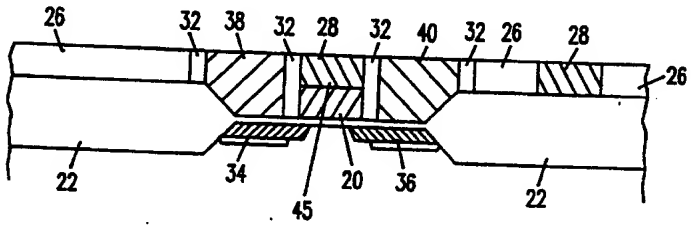


FIG. 5

Pierce teaches that conductive plugs 38, 40 may be formed from (1) deposited polysilicon planarized by chemical mechanical polishing (CMP), (2) polysilicon or single crystal silicon grown by selective chemical vapor deposition (CVD) and doped in situ, or (3) deposited metal(s) planarized by CMP. *Pierce et al*, column 11, lines 12–59. *Pierce* does not teach or suggest that the conductive plugs 38, 40 are source/drain regions, the portion of a metal oxide semiconductor field effect transistor (MOSFET) in which charge carrier (electron or hole) generation or recombination occur. *Pierce* does not teach or suggest doping the conductive

plugs to function as source/drain regions, or in any manner suggest that the conductive plugs are source/drain regions or portions thereof.

The final Office Action asserts that the conductive plugs are indistinguishable from the recited source/drain regions. However, *Pierce* teaches that the conductive plugs 38 and 40 are each a conductor (even if formed of doped semiconductor material), NOT a semiconductor suitable for functioning as source/drain regions. *Pierce* contains no teaching or suggest that plugs 38 and 40 function as anything other than a simple conductor, and only hindsight, with the benefit of Applicants' disclosure, allows recognition that the option of growing single crystal silicon plugs 38, 40 may, if properly doped, allow those regions to serve as a part of the source and drain for the transistor.

In the present invention, the source/drain regions are "wrapped" around the gate by formation of the raised source/drain portions, so that shallow source/drain regions implanted within the substrate may be augmented by the raised source/drain regions. The size of the source/drain regions controls, to some extent, the saturation current and the transconductance of the resulting transistor. *Pierce* contains no teaching or suggestion that the conductive plugs 38, 40 serve as "auxiliary" source/drain regions, only as simple conductors.

Group B

Claims 87 and 90–91 of Group B were rejected under 35 U.S.C. § 103 as obvious over *Pierce* in view of *Doan et al.* These claims are properly grouped together and considered

separately from the claims of Group A since they contain common limitations distinguishing the claims over the cited references not found in the claims of Group A: that the regions implanted within the substrate are lightly doped source/drain regions, while the overlying epitaxial silicon forms the heavily doped source/drain regions.

Claims 87 and 90 of Group B recite that the LDD source/drain regions are the first portions of the source and drain, formed within the substrate, as distinct from the second portion over the first portions. Similarly, claim 88 recites that the second portions (over the substrate) of the source/drain regions are doped to form heavily doped portions, while claim 91 of Group B adds that the first portions (in the substrate) are lightly doped. Such a feature is not shown or suggested by the cited reference.

CONCLUSION

None of the cited references, taken alone or in combination, show or suggest all features of the invention claimed in Groups A–B. Therefore, the rejection under 35 U.S.C. § 103 is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting all pending claims in this application.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 9-23-02

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CLAIMS ON APPEAL

77. (unchanged) An integrated circuit structure, comprising:

a substrate;

a field oxide over the substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate electrode over the surface of the substrate and within the opening, the gate electrode having insulating material on a bottom and on two sides of the gate electrode, wherein the insulating material on the bottom of the gate electrode contacts the substrate; and

source and drain regions adjacent the insulating material on the gate electrode, each source and drain region including

a first portion in the substrate and

a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode.

78. (unchanged) The integrated circuit structure of claim 77, wherein the opening through the substrate has substantially vertical sidewalls.

79. (unchanged) The integrated circuit structure of claim 78, wherein each source and drain region is formed between a sidewall of the opening and the insulating material on the sides of the gate electrode.

80. (unchanged) The integrated circuit structure of claim 79, wherein a space between a sidewall of the opening and the insulating material on the sides of the gate electrode is filled with material forming the second portion of one of the source and drain regions.

81. (unchanged) The integrated circuit structure of claim 77, further comprising:

LDD regions for the source and drain regions formed within the first portion of each source and drain region.

82. (unchanged) The integrated circuit structure of claim 81, wherein the LDD regions are formed in the substrate beneath the insulating material on the sides of the gate electrode.

83. (unchanged) The integrated circuit structure of claim 77, wherein the gate electrode, the insulating material on the sides of the gate electrode, and the second portions of the source and drain regions fill the opening.

84. (unchanged) The integrated circuit structure of claim 77, an upper surface of the gate electrode is further from a surface of the substrate than an upper surface of the field oxide.

85. (twice amended) The integrated circuit structure of claim 77, wherein the first and second portions of the source and drain regions are both formed of a semiconductor material doped to include lightly doped regions within at least the first portions and heavily doped regions within at least the second portions.

86. (unchanged) The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions each form contact regions for source/drain contacts.

87. (unchanged) The integrated circuit structure of claim 82, wherein the LDD regions are the first portions of the source and drain regions.

88. (unchanged) The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions have a dopant concentration suitable for heavily doped source/drain regions.

89. (unchanged) The integrated circuit structure of claim 88, wherein the dopant concentration within the second portions of the source and drain regions is formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

90. (unchanged) The integrated circuit structure of claim 88, wherein the LDD regions are the first portions of the source and drain regions.

91. (unchanged) The integrated circuit structure of claim 88, wherein the first portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

92. (unchanged) The integrated circuit structure of claim 77, further comprising:

a refractory metal silicide on the second portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

93. (unchanged) An integrated circuit structure, comprising:

a field oxide over a substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate structure on the surface of the substrate within the opening, the gate structure having insulating material on a bottom and sides of the gate electrode;

doped regions within portions of the substrate within the opening which are adjacent to and extend beneath the gate structure, wherein the doped regions within the substrate are at least lightly doped; and

doped semiconductor material on the substrate within the opening adjacent to the gate structure and over each of the doped regions within the substrate, the doped semiconductor material doped to a concentration suitable for heavily doped source and drain regions,

wherein the doped regions within the substrate and doped semiconductor material form a source and a drain for a transistor including the gate structure.

94. (unchanged) The integrated circuit structure of claim 93, wherein the doped semiconductor material on the substrate has a dopant concentration formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

95. (unchanged) The integrated circuit structure of claim 93, wherein an upper surface of the doped semiconductor material is coated with a refractory metal silicide to form a contact region to the source and drain.

96. (unchanged) A transistor, comprising:

a gate electrode on an insulating layer over a substrate surface;

insulating sidewall layers on the gate electrode; and

doped source and drain regions within portions of the substrate adjacent to and extending beneath the insulating sidewall layers and within semiconductor material on the substrate adjacent to the insulating sidewall layers,

wherein the portions of the source and drain regions within the substrate are at least lightly doped and the portions of the source and drain regions within the semiconductor material on the substrate are doped to a concentration suitable for heavily doped source and drain regions.